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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,114	09/08/2003	Renat Bilyalov	IMEC285.001AUS	9690

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EXAMINER	
TRINH, THANH TRUC	
ART UNIT	PAPER NUMBER
1795	

NOTIFICATION DATE	DELIVERY MODE
01/21/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/658,114	BILYALOV ET AL.	
	Examiner	Art Unit	
	THANH-TRUC TRINH	1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-26,37-42 and 45-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-26,37-42 and 45-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/14/2008 has been entered.

Remark

2. Claims 1, 3-26, 37-42 and 45-50 are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3-25, 37-42, 45-47 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al.(US Patent 5757024) in view of Berger et al. ("Porosity superlattices: new class of Si heterostructure") .

Regarding claims 1, 3, 40-42, 45-47 and 50, as seen in Figures 2A, 4, 6 and 22C, Yamada et al. teaches a photodiode (or electroluminescent Si-based diode) comprising a first layer (41 and 31 as in Figure 2A, 42and 32 as in Figure 4, 43 as in Figure 6, 404 as in Figure 22C) of first semiconductor material of first conductivity type (or polycrystalline silicon of n-type); second layer (1 as in Figures 2A and 6, 12 as in Figure 4, 403 as in Figure 22C) of second semiconductor material of a second conductivity type (p-type of polycrystalline silicon), wherein the second conductivity type is opposite to the first conductivity type; and a third layer (21 as in Figure 2A, 22 as in Figure 4, 23 as in Figure 6A, and 408 as in Figure 22C) situating between and contacts the first and the second layers (See col. 7 line 55 through col. 12 line 48), wherein the third layer is a single translucent porous layer. Yamada et al. teaches a porous silicon layer situated between two active semiconductor layers (p- and n-type layers), therefore it is the Examiner's position that third layer (or porous semiconductor) is a porous layer of high transparency, a translucent porous layer and also a diffusion barrier.

The difference between Yamada et al. and instant claims is the requirement of the thickness of the third layer (or porous silicon) of from about 1 nm to about 50 nm.

Berger et al. teaches a porous silicon layer used in photodiode (or photoluminescence device) having a thickness of 20 nm (See Figure 1 of Berger et al.).

It would have been obvious to one skilled in the art at the time the invention was made to modify the device of Yamada et al. by having the thickness of the porous silicon (or the third layer) of from about 1 nm to about 50nm as taught by Berger et al., because Berger et al. finds that such thickness would give a porosity having mechanical stability to the layers. (See page 1334)

Regarding claims 4-16, Yamada et al teaches that the first, second and third semiconductor material comprise silicon (See col. 7 line 55 through col. 12 line 48). In other words, they all comprise a same semiconductor material and element.

Regarding claim 17, Yamada et al. teaches the porous silicon layer fabricated from the second layer and has not explicitly been doped (See col. 7 line 55 through col. 12 line 48); therefore it is the Examiner's position that the third layer (or porous silicon layer) comprises a non-doped semiconductor material.

Regarding claims 18-21 and 38, Yamada et al. teaches the porous layer (or third layer) is fabricated from the second layer (1 as in Figures 2A and 6, 12 as in Figure 4, 403 as in Figure 22C) which is polycrystalline silicon semiconductor material (See col. 7 line 55 through col. 12 line 48)

Regarding claim 22, Yamada et al. teaches the first layer (such as layer 41 in Figure 2A) having a thickness of 500 angstroms or 50 nm (See Figure 2A, col. 7 line 67 through col. 8 line 8)

Regarding claim 23, Yamada et al. teaches an amorphous SiO_2 layer (32) is disposed between an n-type silicon layer (42) and a porous silicon layer (22). (See Figure 4, col. 8 lines 47-51).

Regarding claims 24-25, Berger et al. teaches a photoluminescence device (or photodiode) comprising a lattice structure of porous silicon layers formed from a p-type silicon substrate (similar to the second layer of Yamada et al.); wherein the fourth layer (e.g. a first porous Si layer of either type I or II) attached to the second layer (or the substrate), and the fifth layer is the next porous Si layer of either type II or I) attached to the fourth layer. (See the whole document of Berger et al.)

Regarding claim 37, Berger et al. teaches a porous silicon layer with 20 nm thick has 64% porosity. (See Figure 1 of Berger et al.)

Regarding claim 39, Yamada et al. teaches a photodiode (or electroluminescent Si-based diode) comprising a first layer (41 as in Figure 2A, 42 as in Figure 4, 43 as in Figure 6, 404 as in Figure 22C) of first semiconductor material of first conductivity type (or polycrystalline silicon of n-type); second layer (1 as in Figures 2A and 6, 12 as in Figure 4, 403 as in Figure 22C) of second semiconductor material of a second conductivity type (p-type of polycrystalline silicon), wherein the second conductivity type is opposite to the first conductivity type; and a third layer (21 as in Figure 2A, 22 as in Figure 4, 23 as in Figure 6A, and 408 as in Figure 22C) situating between the first and the second layers (See col. 7 line 55 through col. 12 line 48). Yamada et al. also teaches the porous silicon layer (or third layer) is fabricated from the second layer of polycrystalline silicon and has not explicitly been doped (See col. 7 line 55 through col. 12 line 48). Yamada et al. further teaches polycrystalline silicon including amorphous silicon (See col. 21 lines 34-38). Therefore it is also the Examiner's position that Yamada et al. teaches the second layer comprises a mulitcrystalline (or polycrystalline)

silicon semiconductor material of p-type conductivity, the first layer comprises an amorphous silicon semiconductor material of n-type conductivity, and the third layer consists of a porous non-doped silicon semiconductor material.

4. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. in view of Berger et al. and further in view of Suzuki et al. (US Patent 5644156)

Yamada et al. in view of Berger et al. teaches a photodiode as applied to claims 3-25, 37-42 and 45-47.

Yamada et al. in view of Berger et al. does not specifically teach the second layer comprises a plurality of macro etch pits comprising a diameter of greater than about one micron, and wherein a portion of the macro etch pits comprise a plurality of fine etch pits comprising a diameter of less than about one micron.

Suzuki et al. teaches a photodiode comprising a first layer (251) of p-type conductivity, a second layer (252) of n-type conductivity (See Figures 42-45; col. 35 lines 30 to col. 38 line 8), wherein the second layer comprises a sponge-like structure with pores having diameters from a few nanometers to a few tens of micrometers (See col. 36 lines 50-56). Therefore it is the Examiner's position that Suzuki et al. teaches the second layer comprises a plurality macro etch pits having diameters of greater than about one micron, and wherein a portion of the macro etch pits comprise a plurality of fine etch pits having diameter of less than about one micron.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Yamada et al. in view of Berger et al. by

forming on the second layer a plurality of macro etch pits (or sponge-like structure) comprising diameter of greater than about one micron with a portion comprising a plurality of etch pits having diameter of less than about one micron as taught by Suzuki et al., because Suzuki et al. teaches that forming a plurality etch pits would provide stable luminescence characteristics. (See col. 35 lines 44-52).

5. Claim 48-49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. in view of Berger et al. and further in view of Fonash et al. (US Patent 6399177)

Yamada et al. in view of Berger et al. teaches a photodiode as applied to claims 3-25, 37-42 and 45-47.

Yamada et al. in view of Berger et al. does not teach the third layer consists of germanium or carbon.

Fonash et al. teaches a porous structure (similar to the instant third layer) that has a photovoltaic properties is formed on a semiconductor substrate (See Figure 12a, col. 6 line 65 through col. 8 line 41, claim 22 of Fonash et al.), wherein the porous structure is made of silicon, germanium, or carbon. (See claim 10 of Fonash et al.).

It would have been obvious to one skilled in the art at the time the invention was made to modify the device of Yamada et al. in view of Berger et al. by using materials such as germanium or carbon to form the porous layer (or instant third layer) as taught by Fonash et al., because Fonash et al. finds materials such as germanium and carbon are suitable materials for forming a porous layer. (See claims 1 and 10 of Fonash et al.)

Response to Arguments

Applicant's arguments filed 11/14/2008 have been fully considered but they are not persuasive.

Applicant argues that Berger et al. teaches porous superlattices comprising alternative regions with high and low porosity and the total thickness of the superlattices is 1.5 micrometers, not from about 1 nm to about 5 nm as recited in claim 1. However, the Examiner respectfully disagrees. Yamada et al. teaches a single porous layer, and Berger et al. teaches a single porous layer used in photoluminescence device having a thickness of 20 nm (See Figure 1 of Berger et al.).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THANH-TRUC TRINH whose telephone number is (571)272-6594. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nam X Nguyen/
Supervisory Patent Examiner, Art Unit 1753

TT
12/08/2008